a memory module;

a battery of input/output registers connected to the memory module by a two-way link;

an input register for receiving the data elements of a message to be processed by an encryption or decryption operation;

a key register for receiving the data elements of an encryption or decryption digital key for use in the encryption or decryption operation;

a multiplexer to carry out a transfer of data between the battery of input/output registers and the input register and the key register;

a processing module to perform the encryption or decryption operation and for receiving the message to be processed from the input register and for receiving the digital key from the key register to process the message;

a control module for controlling the memory module, the battery of input/output registers, the multiplexer and the processing module; and

an output register to transmit the result of the encryption or decryption operation to the battery of input/output registers through the multiplexer;

the battery of input/output registers comprising a scrambling register to receive scrambling bits foreign to the message to be processed or to the digital key.

12. An electronic circuit according to Claim 11 wherein the scrambling bits are foreign to the message to be processed and to the digital key.

13. An electronic circuit according to Claim 11, further comprising an accessory input register connected to

the processing module and to the multiplexer to receive the scrambling bits from the processing module or from the memory module.

14. An electronic circuit according to Claim 13, wherein the accessory input register is the same size as the scrambling register.

15. An electronic circuit according to Claim 11, wherein the scrambling bits are generated randomly.

16. An electronic circuit according to Claim 11, wherein the scrambling bits are sent in groups of eight bits.

17. An electronic circuit for a cryptography coprocessor comprising:

a plurality of input/output registers having a scrambling register for receiving scrambling bits;

an input register for receiving message data to be processed by an encryption or decryption operation;

a key register for receiving encryption or decryption key data for use in the encryption or decryption operation;

a multiplexer for transferring data between the plurality of input/output registers and the input register and the key register;

a processor for performing the encryption or decryption operation and for receiving the message data from the input register and for receiving the key data from the key register;

a controller for controlling the plurality of input/output registers, the multiplexer and the processor; and

an output register to transmit the result of the encryption or decryption operation to the plurality of input/output registers through the multiplexer.

18. An electronic circuit according to Claim 17 wherein the scrambling bits are foreign to the message data and the key data.

19. An electronic circuit according to Claim 17, further comprising an accessory input register connected to the processing module and to the multiplexer to receive the scrambling bits from the processing module.

20. An electronic circuit according to Claim 19, wherein the accessory input register is the same size as the scrambling register.

21. An electronic circuit according to Claim 17, further comprising:

a memory connected to the plurality of input/output registers; and

an accessory input register connected to the processing module and to the multiplexer for receiving the scrambling bits from the memory.

22. An electronic circuit according to Claim 21, wherein the accessory input register is the same size as the scrambling register.

23. An electronic circuit according to Claim 17, wherein the scrambling bits are generated randomly.

24. An electronic circuit according to Claim 17, wherein the scrambling bits are sent in groups of eight bits.

25. A method for securing a cryptography coprocessor comprising the steps of:

transmitting data by a two-way link from a memory module to a battery of input/output registers;

transmitting data corresponding to a message to be processed by an encryption or decryption operation, through a multiplexer, from the battery of input/output registers to an input register; and

transmitting data corresponding to an encryption or decryption digital key for the encryption or decryption operation, through the multiplexer, from the battery of input/output registers to a key register;

transmitting scrambling bits, which are foreign to the message to be processed, with the digital key, to a scrambling register of the battery of input/output registers from the memory module or the processing module; and

processing the message to be processed with a processing module receiving the data from the input register, receiving the data from the key register, and outputting the data corresponding to the processed message to an output register.

26. A method according to Claim 25, wherein the scrambling bits are transmitted into an accessory register connected to the processing module and to the multiplexer to receive the scrambling bits from the processing module or from the memory module.

27. A method according to Claim 25, wherein the scrambling bits are transmitted randomly.

28. A method according to Claim 25, wherein the scrambling bits are transmitted to the scrambling register whenever a digital key is input into the battery of input/output registers.

29. A method according to Claim 25, wherein the scrambling bits comprise groups of eight bits.

30. A method for operating a cryptography coprocessor comprising the steps of:

transmitting data to a plurality of input/output registers;

transmitting message data to be processed by an encryption or decryption operation, through a multiplexer, from the plurality of input/output registers to an input register; and

transmitting key data for the encryption or decryption operation, through the multiplexer, from the plurality of input/output registers to a key register;

transmitting scrambling bits to a scrambling register of the plurality of input/output registers; and

processing the message data with a processor receiving the data from the input register, receiving the data from the key register, and outputting the corresponding message data to an output register.

31. A method according to Claim 30 wherein the scrambling bits are transmitted into an accessory register